IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A memory hub, comprising:

a first ingress interface for receiving from a source port packets having associated ingress flows and assigning ingress flow values to the packets associated with the ingress flows that identify packets having similar ~~Quality~~ Class of Service processing requirements and storing the packets in an ingress memory;

a second ingress interface for outputting packets or cells to a switch fabric connecting the first and second ingress interface to an egress interface and egress memory; and

an ingress controller that queues the packets or cells in the ingress memory for sending to the egress memory via the switch fabric according to the ~~Quality~~ Class of Service processing requirements identified by the associated ingress flow values.

2. (Previously presented) A memory hub according to claim 1 including an ingress traffic manager that schedules how the packets or cells are output to the switch fabric, the traffic manager modifying an assigned Class of Service for the packets and assigning the modified Class of Service to the packets before being output to the switch fabric.

3. (Previously presented) A memory hub according to claim 2 wherein the ingress traffic manager schedules outputting of the packets or cells to the switch fabric on a per Class of Service basis or per destination basis.

4. (Original) A memory hub according to claim 2 wherein the ingress controller manages memory operations for queuing the packets or cells independently of controls from the ingress traffic manager.

5. (Currently amended) A memory hub according to claim [[4]] 2 wherein the ingress controller and the ingress traffic manager are separate circuits operating on separate integrated circuits.

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6. (Original) A memory hub according claim 1 including a Class of Service queuer that receives packets or cells output from the second ingress interface on a per flow basis and sends the packets or cells to the switch fabric on a per Class of Service associated basis.

7. (Original) A memory hub according to claim 2 wherein the ingress traffic manager directs the ingress controller to drop packets or cells for ingress flows that back up.

8. (Previously presented) A memory hub according to claim 1 wherein the ingress flow values are assigned independently of the source port receiving the packets.

9. (Original) A memory hub according to claim 1 including egress flow fields for assigning egress flow Ids to the packets or cells according to the associated ingress flows.

10. (Original) A memory hub according to claim 1 including forwarding label fields for assigning forwarding labels to the packets or cells according to the associated ingress flows.

11. (Original) A memory hub according to claim 10 wherein the forwarding label fields contain information for establishing a path in the switching fabric to a destination port.

12. (Previously presented) A memory hub according to claim 1 wherein the memory hub is an integrated circuit having a first interface for communicating with one or more source ports, a second interface for communicating with an ingress traffic manager, a third interface for communicating with a switch fabric and a fourth interface for communicating with an external memory.

13. (Previously presented) A memory hub according to claim 1 including:

an egress controller having a first interface for receiving packets or cells output from the switch fabric having associated egress flows;

a second interface for transferring the packets to a destination port; and

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an egress controller configured to manage how the packets are queued to the destination port according to the associated egress flows, the egress controller tracking packet size information for the egress flows and queuing the packets for outputting to destination ports according to the tracked packet size information.

14. (Original) A memory hub according to claim 13 including egress queues for maintaining pointers to the packets or cells received from the switch fabric according the associated egress flows.

15. (Original) A memory hub according to claim 14 including forwarding label fields for identifying forwarding labels for the egress queues.

16. (Original) A memory hub according to claim 15 wherein the forwarding label fields identify source ports.

17. (Previously presented) A memory hub according to claim 1 wherein the first ingress interface stores the packets in an external ingress memory and the second ingress interface outputs the packets from the external ingress memory through the switch fabric to an external egress memory according to the ingress flow values associated with the packets.

18. (Original) A memory hub according to claim 13 including an egress traffic manager that receives egress flow information from the egress controller and schedules the egress controller to output packets to the destination port according to the egress flow information.

19. (Original) A memory hub according to claim 14 wherein the egress traffic manager notifies the egress memory hub to drop packets or cells for egress queues that back up.

20. (Previously presented) A method for forwarding packets in a network processing device, comprising:

receiving packets associated with ingress flows;

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assigning internal ingress flow ID values to the packets that identify packets having similar processing requirements, assigning the internal flow ID values independently of source addresses or destination addresses associated with the packets;

queuing the packets for sending to an egress queue according to the associated ingress flow Id values;

outputting the queued packets to an egress memory hub according to the ingress flow ID values.

21. (Original) A method according to claim 20 including managing memory operations for queuing the packets in a first integrated circuit and independently managing in a second integrated circuit how the queued packets are scheduled for being output.

22. (Previously presented) A method according to claim 20 including assigning the ingress flow ID values to the packets on a per Class of Service basis independently of an ingress port receiving the packets and an egress port outputting the packets.

23. (Previously presented) A method according to claim 20 including outputting the queued packets on a per flow basis and requeuing the output packets for outputting to a switch fabric for sending to an egress memory on a per Class of Service basis.

24. (Original) A method according to claim 20 including identifying egress flows for the ingress flows and assigning the identified egress flows to the packets before being output.

25. (Previously presented) A method according to claim 20 including queuing the packets for sending over a switch fabric to an egress queue according to the ingress flow ID values and then re-queuing the packets in the egress queue for outputting over an external network interface according to the ingress flow ID values.

26. (Original) A method according to claim 20 including identifying a Class of Service for the ingress flows and assigning the Class of Service to the packets before being output to the switch fabric.

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27. (Previously presented) A method for forwarding packets in a network processing device, comprising:

receiving packets associated with ingress flows;

queuing the packets according to the associated ingress flows;

identifying ingress flow information for the packets;

outputting the queued packets according to the ingress flow information;

identifying a Class of Service for the ingress flows and assigning the Class of Service to the packets before being output to the switch fabric; and

modifying the assigned Class of Service and assigning the modified Class of Service to the packets before being output.

28. (Original) A method according to claim 20 including tracking ingress flow information for the packets and scheduling the packets for outputting to a switch fabric according to the tracked ingress flow information.

29. (Original) A method according to claim 28 including dropping queued packets when a back up is indicated by the tracked ingress flow information.

30. (Original) A method according to claim 20 including receiving the packets with associated egress flows from a switch fabric and queuing the packets for outputting to destination ports according to the egress flows.

31. (Original) A method according to claim 30 including associating forwarding labels and ingress flows with the egress flows for the packets received from the switch fabric.

32. (Previously presented) A method for forwarding packets in a network processing device, comprising:

receiving packets associated with ingress flows;

queuing the packets according to the associated ingress flows;

identifying ingress flow information for the packets;

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outputting the queued packets according to the ingress flow information;

receiving the packets with associated egress flows from a switch fabric and queuing the packets for outputting to destination ports according to the egress flows;

associating forwarding labels and ingress flows with the egress flows for the packets received from the switch fabric; and

identifying egress flows that are backing up and notifying source ports causing the back up using the ingress flows and forwarding labels associated with the identified egress flows.

33. (Original) A method according to claim 20 including identifying unused egress queues for each egress port associated with a multicast packet, using a common CAM value to map to the unused egress queues in each egress port, and assigning the CAM value to the multicast packet as an egress flow value.

34. (Original) A method according to claim 33 including:

receiving the multicast packet from a switch fabric;

using the CAM value in the multicast packet to access a content addressable memory; and

using an egress queue mapped by the content addressable memory as the egress queue for the multicast packet.

35. (Previously presented) A method for forwarding packets in a network processing device, comprising:

receiving packets associated with ingress flows;

queuing the packets according to the associated ingress flows;

identifying ingress flow information for the packets;

outputting the queued packets according to the ingress flow information;

identifying egress flows for the ingress flows and assigning the identified egress flows to the packets before being output; and

tracking packet size information for the egress flows and queuing the packets for outputting to destination ports according to the tracked packet size information.

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36. (Original) A method according to claim 20 including providing an Egress flow Id, Class of Service, or forwarding label value with the received packets.

37. (Original) A method according to claim 20 including providing an Egress flow Id, Class of Service, or forwarding label value in a memory hub data structure.

38. (Currently amended) A memory hub, comprising:

a first interface for receiving packets or packet fragments having associated flow Ids;

a second interface for outputting the packets or packet fragments;

a third interface for communicating with another memory hub; and

a controller that queues the packets or packet fragments in a memory according to the associated flow Ids and dequeues the packets from the memory according to the associated flow Ids.

39. (Currently amended) A memory hub ~~according to claim~~, comprising:

a first interface for receiving packets or packet fragments having associated flow Ids;

a second interface for outputting the packets or packet fragments;

a controller that queues the packets or packet fragments in a memory according to the associated flow Ids and dequeues the packets from the memory according to the associated flow Ids;

wherein the memory hub is an integrated circuit with the first interface receiving the packets or packet fragments from a source port, the second interface outputting the packets or packet fragments to a switch fabric and including[[:]]

a third interface communicating with the controller and a fourth interface communicating with an external memory.

40. (Original) A memory hub according to claim 38 wherein the first interface receives the packets or packet fragments from a switch fabric and the second interface outputs packets to an egress packet processor.

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41. (Currently amended) A memory hub ~~according to claim 40 including~~, comprising:

a first interface for receiving packets or packet fragments having associated flow Ids;

a second interface for outputting the packets or packet fragments;

a controller that queues the packets or packet fragments in a memory according to the associated flow Ids and dequeues the packets from the memory according to the associated flow Ids;

wherein the first interface receives the packets or packet fragments from a switch fabric and the second interface outputs packets to an egress packet processor; and

another memory hub having a first interface configured to receive packets from the egress packet processor and a second interface configured to output packets to an egress interface.

42. (Currently amended) A memory hub ~~according to claim 40 including~~, comprising:

a first interface for receiving packets or packet fragments having associated flow Ids;

a second interface for outputting the packets or packet fragments;

a controller that queues the packets or packet fragments in a memory according to the associated flow Ids and dequeues the packets from the memory according to the associated flow Ids;

wherein the first interface receives the packets or packet fragments from a switch fabric and the second interface outputs packets to an egress packet processor; and

a traffic manager that receives packet lengths associated with the packets output from the egress packet processor.

43. (Currently amended) A memory hub ~~according to claim 40 including~~, comprising:

a first interface for receiving packets or packet fragments having associated flow Ids;

a second interface for outputting the packets or packet fragments;

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a controller that queues the packets or packet fragments in a memory according to the associated flow Ids and dequeues the packets from the memory according to the associated flow Ids;

wherein the first interface receives the packets or packet fragments from a switch fabric and the second interface outputs packets to an egress packet processor; and

a traffic manager that receives packet lengths associated with the packets received from the first interface.

44. (Previously presented) A memory hub, comprising:

a first interface for receiving packets or packet fragments having associated flow Ids;

a second interface for outputting the packets or packet fragments;

a controller that queues the packets or packet fragments in a memory according to the associated flow Ids and dequeues the packets from the memory according to the associated flow Ids; and

a third interface configured to receive the packets with updated packet headers back from the egress packet processor and a fourth interface for outputting the updated packets to an egress interface circuit.

45. (Currently amended) A memory hub ~~according to claim 38~~, comprising:

a first interface for receiving packets or packet fragments having associated flow Ids;

a second interface for outputting the packets or packet fragments;

a controller that queues the packets or packet fragments in a memory according to the associated flow Ids and dequeues the packets from the memory according to the associated flow Ids;

wherein the packets or packet fragments include an egress flow Id, Class of Service, or forwarding label value.

46. (Currently amended) A memory hub ~~according to claim 38 including~~, comprising:

a first interface for receiving packets or packet fragments having associated flow Ids;

a second interface for outputting the packets or packet fragments;

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a controller that queues the packets or packet fragments in a memory according to the associated flow Ids and dequeues the packets from the memory according to the associated flow Ids; and

a data structure that includes an egress flow Id, Class of Service, or forwarding label value.

47. (Currently amended) A memory hub ~~according to claim 38~~, comprising:

a first interface for receiving packets or packet fragments having associated flow Ids;

a second interface for outputting the packets or packet fragments;

a controller that queues the packets or packet fragments in a memory according to the associated flow Ids and dequeues the packets from the memory according to the associated flow Ids;

wherein the controller tracks packet size information for the flow Ids and queues the packets for outputting to destination ports according to the tracked packet size information.

48. (New) A memory hub according to claim 38 wherein

the third interface communicates with an ingress memory hub when operating in an egress memory hub.

49. (New) A memory hub according to claim 48 wherein the third interface communicates with an egress memory hub when operating in an ingress memory hub.

50. (New) A memory hub according to claim 48 wherein the first interface receives the packets or packet fragments from a switch fabric and the second interface outputs packets to an egress packet processor.

51. (New) A memory hub according to claim 38, wherein the third interface is used for sending information related to forwarding labels, ingress flow Id's, and control packets.

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